

B1 delivering the pre-fetched data from the cache queue to a bus independently of the memory.

1 2. The method of claim 1 wherein pre-fetching comprises:  
2 determining if an amount of data in the cache queue is above a predetermined level; and  
3 placing the request to a memory controller controlling the memory if the amount of data  
4 is not above the predetermined level, the request causing the memory controller to transfer the  
5 plurality of data to the cache queue, the request being buffered in a request queue.

1 3. The method of claim 2 wherein the delivering comprises:  
2 transferring the data from the cache queue to the bus if the data in the cache queue is  
3 ready.

1 4. The method of claim 1 further comprising:  
2 determining if the request is valid; and  
3 processing a cache miss request if the request results in a cache miss.

1 5. The method of claim 4 wherein the processing of the cache miss request  
2 comprises:  
3 providing a purge signal;  
4 marking an entry in a scheduler according to the purge signal;  
5 purging data corresponding to the marked entry; and  
6 placing the request to the memory controller.

1 6. The method of claim 5 wherein the bus is a peripheral component interconnect  
2 (PCI) bus.

1 7. The method of claim 6 wherein the request is one of a 32-byte and a 64-byte  
2 requests.

B2 1 8. (AMENDED) An apparatus comprising:  
2 a pre-fetcher to pre-fetch a plurality of data from a memory to a cache queue in response  
3 to a request; and

B2

4 a cache controller coupled to the cache queue and the pre-fetcher to deliver the pre-  
5 fetched data from the cache queue to the bus independently of the memory.

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1 9. The apparatus of claim 8 wherein the pre-fetcher comprises:  
2 a watermark monitor to determine if an amount of data in the cache queue is above a  
3 predetermined level;  
4 a request packet generator coupled to the watermark monitor to place the request to a  
5 memory controller controlling the memory if the amount of data is not above the predetermined  
6 level, the request causing the memory controller to transfer the plurality of data to the cache  
7 queue; and  
8 a request queue coupled to the request packet generator to store the request provided by  
9 the request packet generator.

1 10. The apparatus of claim 9 wherein the cache controller transfers the data from the  
2 cache queue to the bus if the data in the cache queue is ready.

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B3

1 11. (AMENDED) The apparatus of claim 9 further comprising:  
2 a peripheral bus controller coupled to the bus and the pre-fetcher to determine if the  
3 request is valid;  
4 a data coherence controller coupled to the pre-fetcher to provide a purge signal when the  
5 request corresponds to a cache miss; and  
6 a scheduler coupled to the request queue and the data coherence controller to store entries  
7 corresponding to the request, the entries being marked according to the purge signal from the  
8 data coherence controller.

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1 12. The apparatus of claim 11 further comprising:  
2 a data mover coupled to the cache queue and the scheduler to transfer data from the  
3 memory to the cache queue, the data mover purging data corresponding to a marked entry from  
4 the scheduler.

1 13. The apparatus of claim 12 wherein the bus is a peripheral component interconnect  
2 (PCI) bus.

1 14. The apparatus of claim 13 wherein the request is one of a 32-byte and a 64-byte  
2 requests.

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1 15. (AMENDED) A system comprising:  
2 a memory;  
3 a bus; and  
4 a bus access circuit coupled to the memory and the bus to reduce latency in accessing the  
5 memory from the bus, the bus access circuit including:  
6 a pre-fetcher to pre-fetch a plurality of data from the memory to a cache queue in  
7 response to a request, and  
8 a cache controller coupled to the cache queue and the pre-fetcher to deliver the  
9 pre-fetched data from the cache queue to the bus independently of the memory.

1 16. (AMENDED) The system of claim 15 wherein the pre-fetcher comprises:  
2 a watermark monitor to determine if an amount of data in the cache queue is above a  
3 predetermined level;  
4 a request packet generator coupled to the watermark monitor to place the request to a  
5 memory controller controlling the memory if the amount of data is not above the predetermined  
6 level, the request causing the memory controller to transfer the plurality of data to the cache  
7 queue; and  
8 a request queue coupled to the request packet generator to store the request provided by  
9 the request packet generator.

1 17. The system of claim 16 wherein the cache controller transfers the data from the  
2 cache queue to the bus if the data in the cache queue is ready.

B5  
1 18. (AMENDED) The system of claim 16 wherein the bus access circuit further  
2 comprises:  
3 a peripheral bus controller coupled to the bus and the pre-fetcher to determine if the  
4 request is valid;  
5 a data coherence controller coupled to the pre-fetcher to provide a purge signal when the  
6 request corresponds to a cache miss; and

b5

7 a scheduler coupled to the request queue and the data coherence controller to store entries  
8 corresponding to the request, the entries being marked according to the purge signal from the  
9 data coherence controller.

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1 19. The system of claim 18 wherein the bus access circuit further comprising:  
2 a data mover coupled to the cache queue and the scheduler to transfer data from the  
3 memory to the cache queue, the data mover purging data corresponding to a marked entry from  
4 the scheduler.

1 20. The system of claim 19 wherein the bus is a peripheral component interconnect  
2 (PCI) bus.

1 21. The system of claim 20 wherein the request is one of a 32-byte and a 64-byte  
2 requests.

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